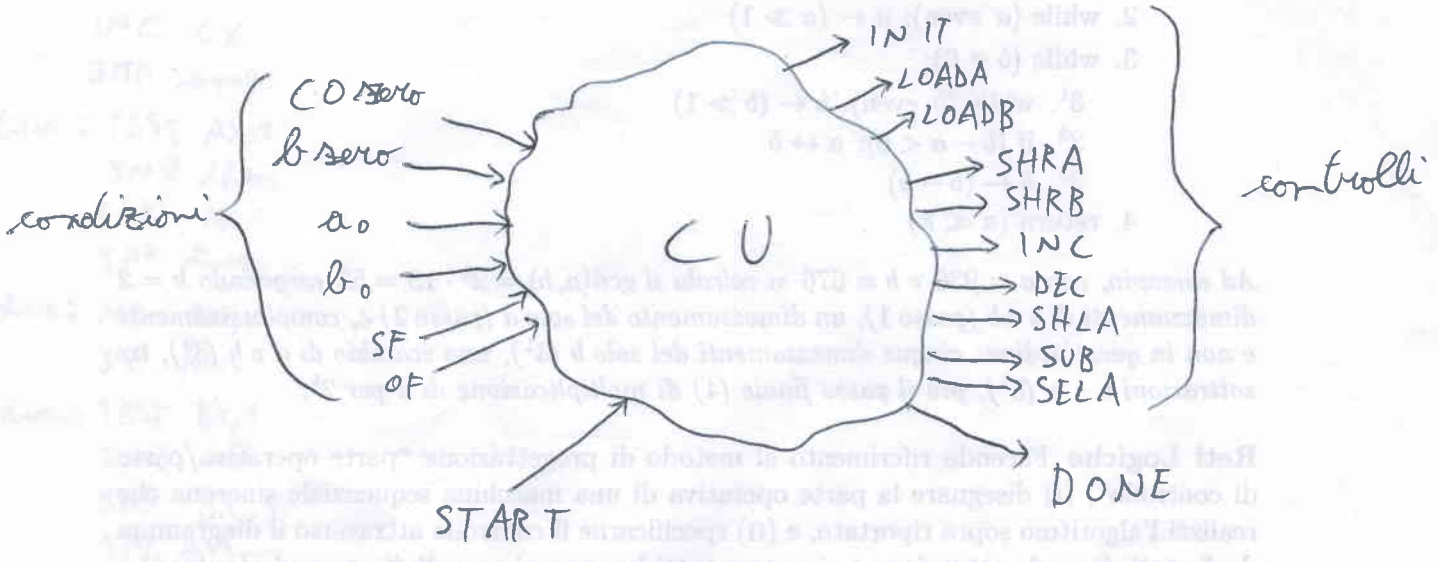
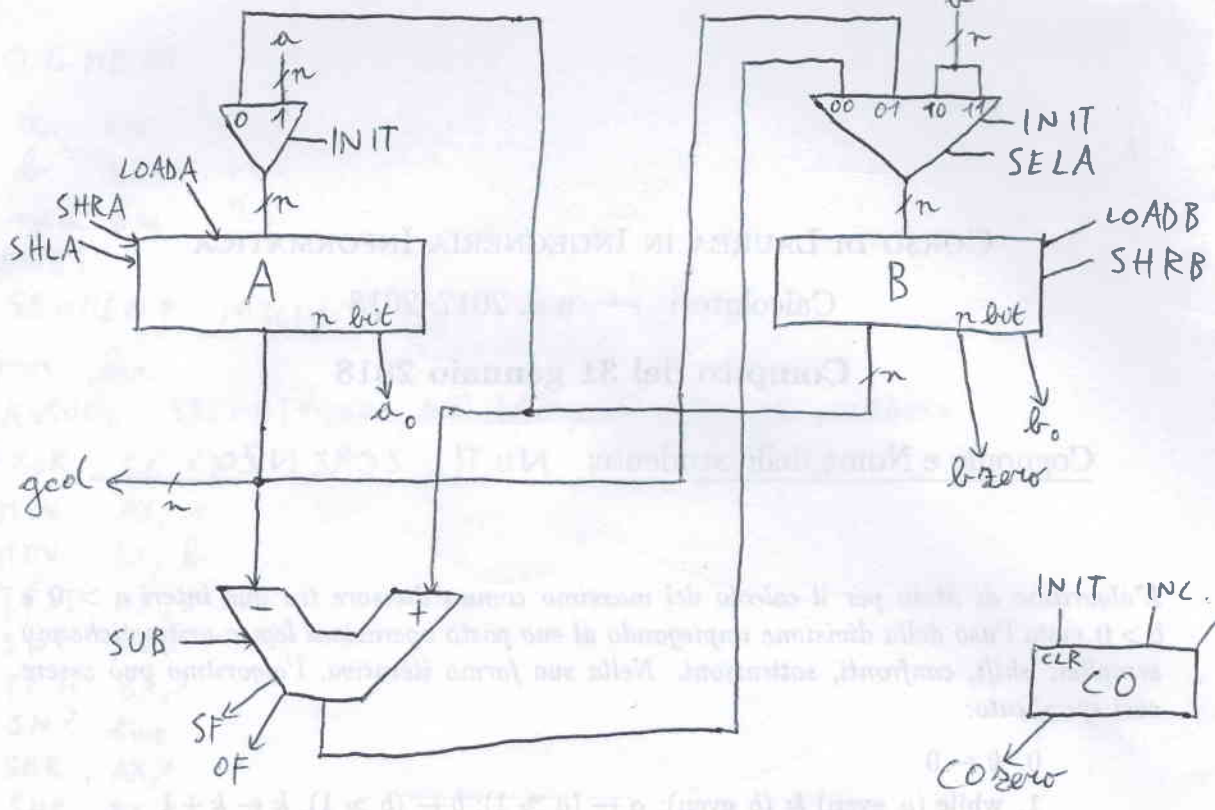
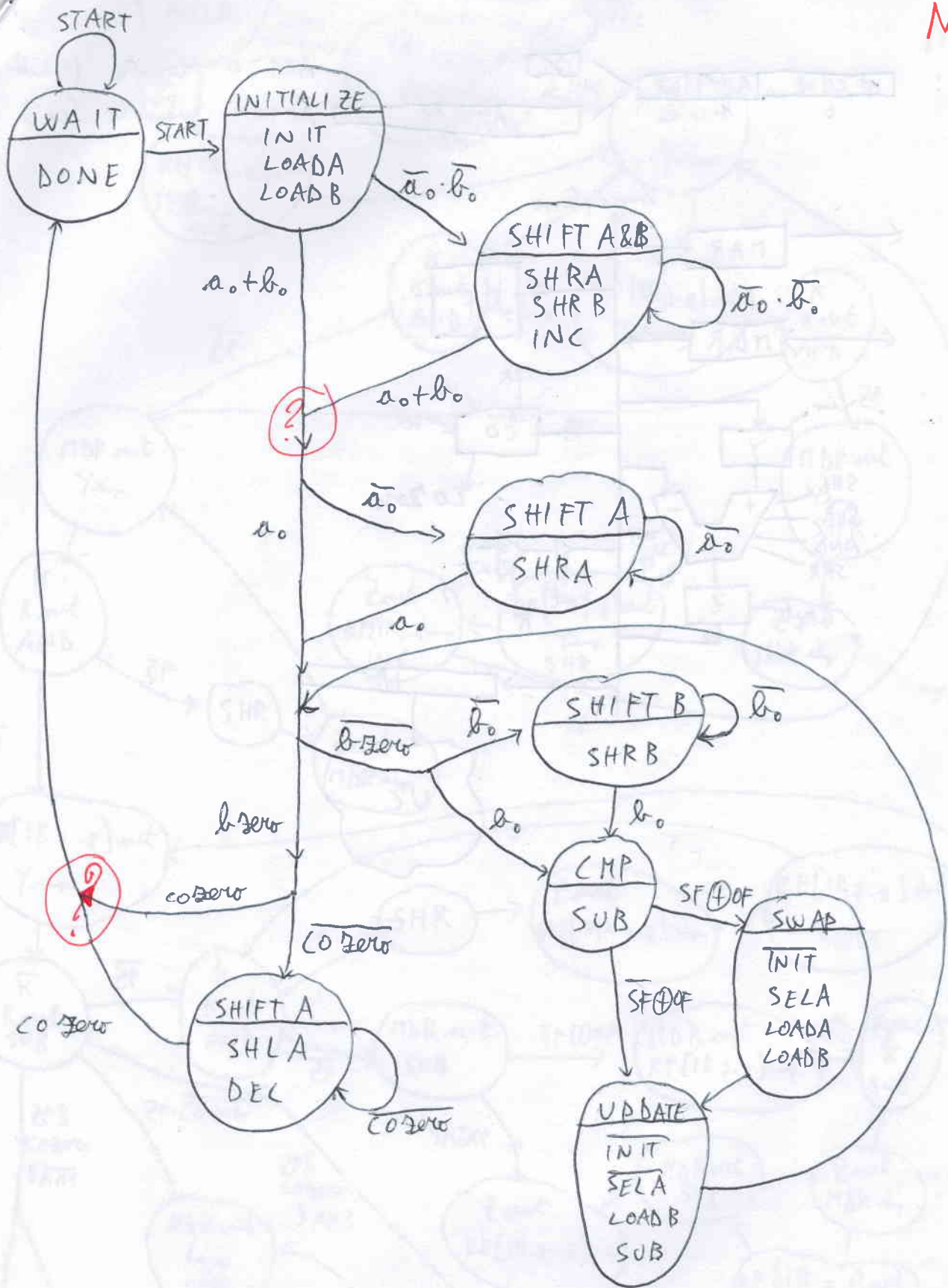


es 7

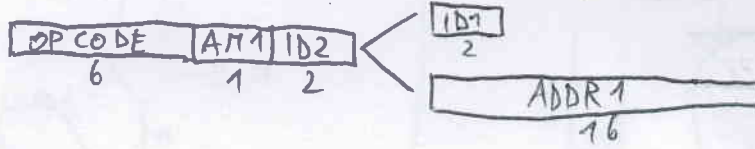




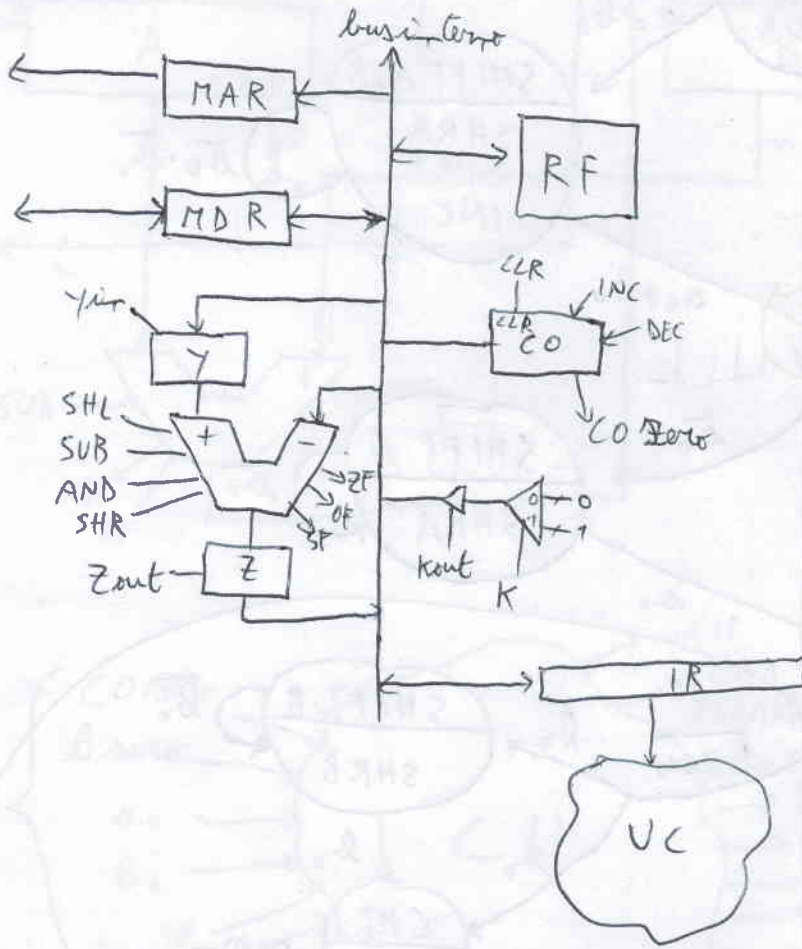
? Uso di una notazione semplificata, e non totalmente soddisfacente, che mira a ridurre il numero di archi tra uno stato e l'altro. Dove si incontrano due archi è come se ci fosse uno stato dove si fonde un colpo di clock solo per cambiare gli ingressi, senza cioè produrre alcuna uscita.

es 2) *full*

codifica:

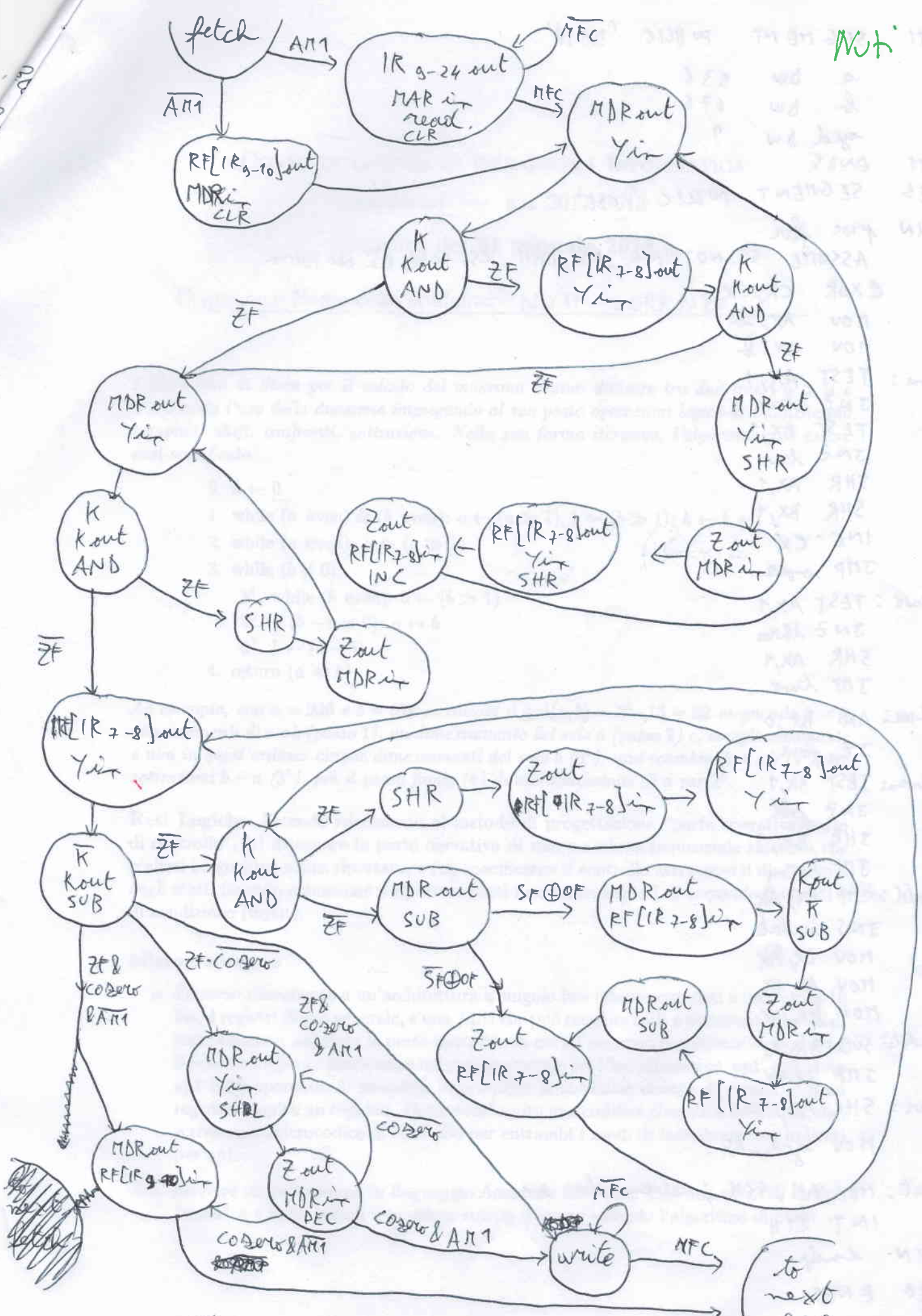


AN1=0 registro (registro)
AN1=1 memoria (zaicki feta)



Handwritten notes at the bottom of the page, partially obscured and difficult to read.

NOT



Il risultato viene messo in q01

to next fetch

DATI SEGMENT PUBLIC 'DATA'

a DW 936

b DW 676

gcd DW ?

DATI ENDS

CSEG SEGMENT PUBLIC 'CODE'

MAIN PROC far

ASSUME SS: NOTHING, DS: DATI, CS: CODE, ES: NOTHING

EXOR CX, CX

MOV AX, a

MOV BX, b

one: TEST AX, 1

JNZ two

TEST BX, 1

JNZ two

SHR AX, 1

SHR BX, 1

INC CX

JMP one

two: TEST AX, 1

JNZ three

SHR AX, 1

JMP two

three: ADD BX, 0

JZ four

even: TEST BX, 1

JNZ odd

SHR BX, 1

JMP even

odd: CMP BX, AX

JNS update

MOV DX, AX

MOV AX, BX

MOV BX, DX

update: SUB BX, AX

JMP three

four: SHL AX, CX

MOV gcd, AX

exit: MOV AH, 4CH ; return to o.s.

INT 21H

MAIN ENDP

CSEG ENDS

END MAIN