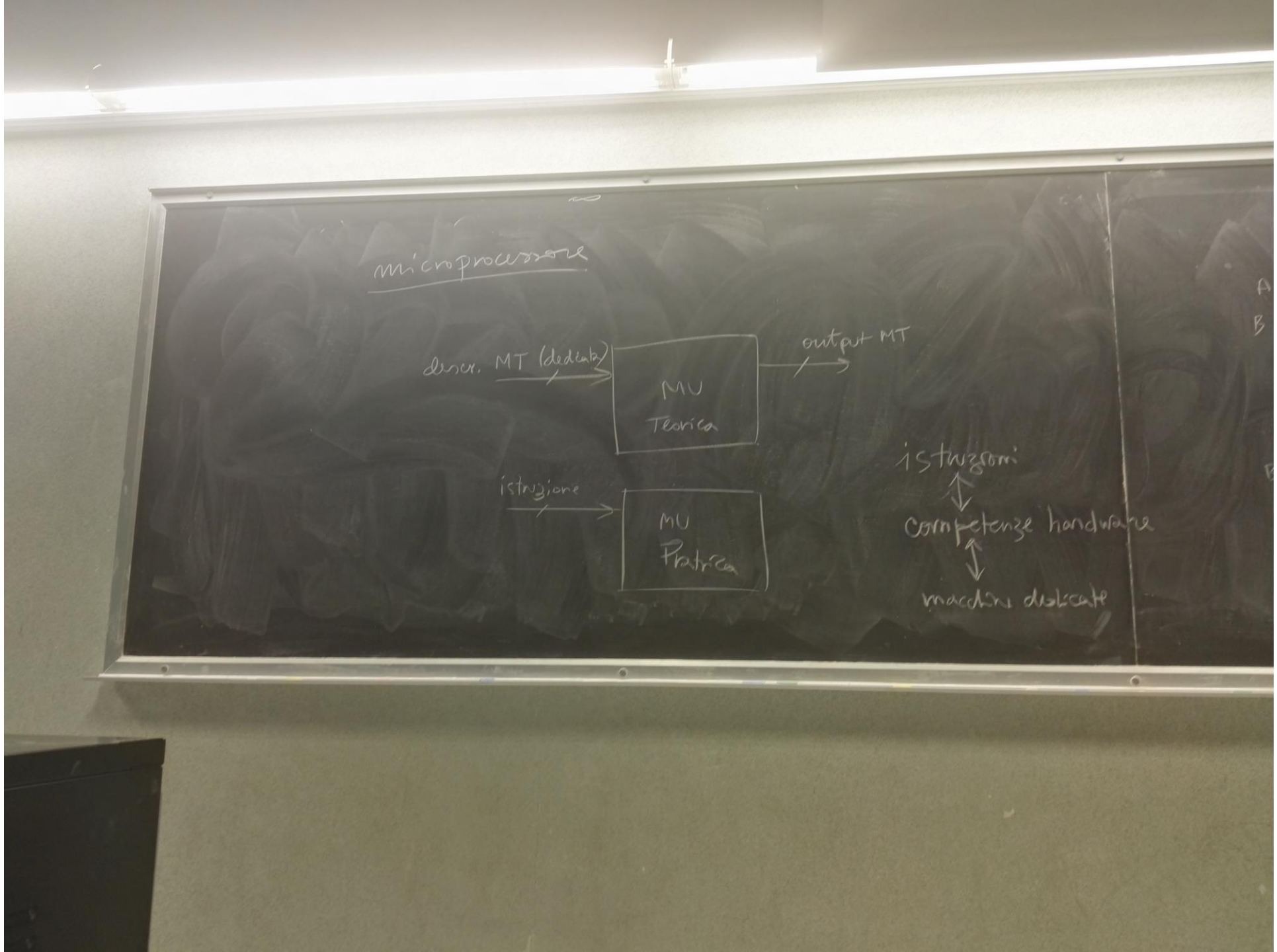
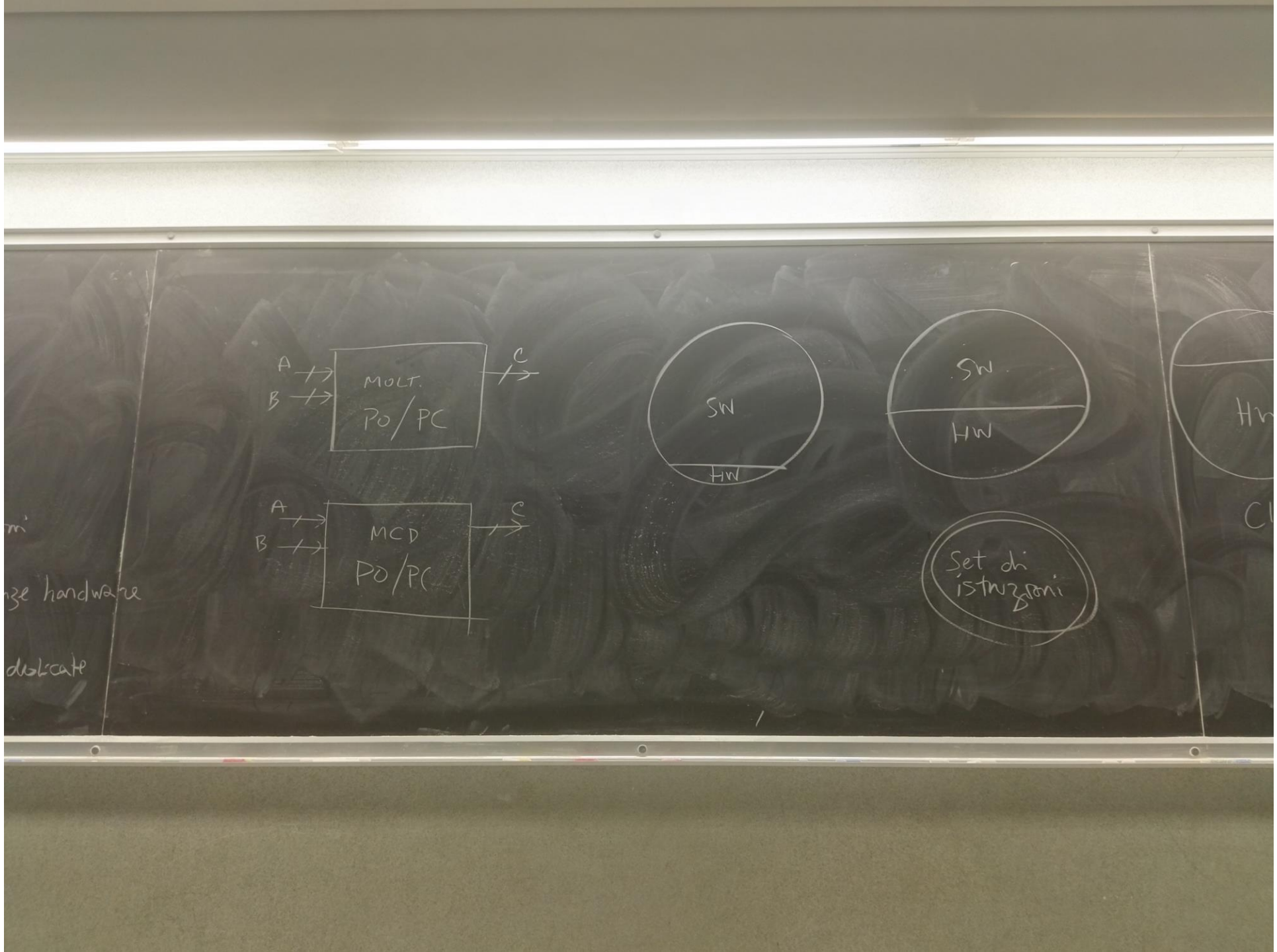
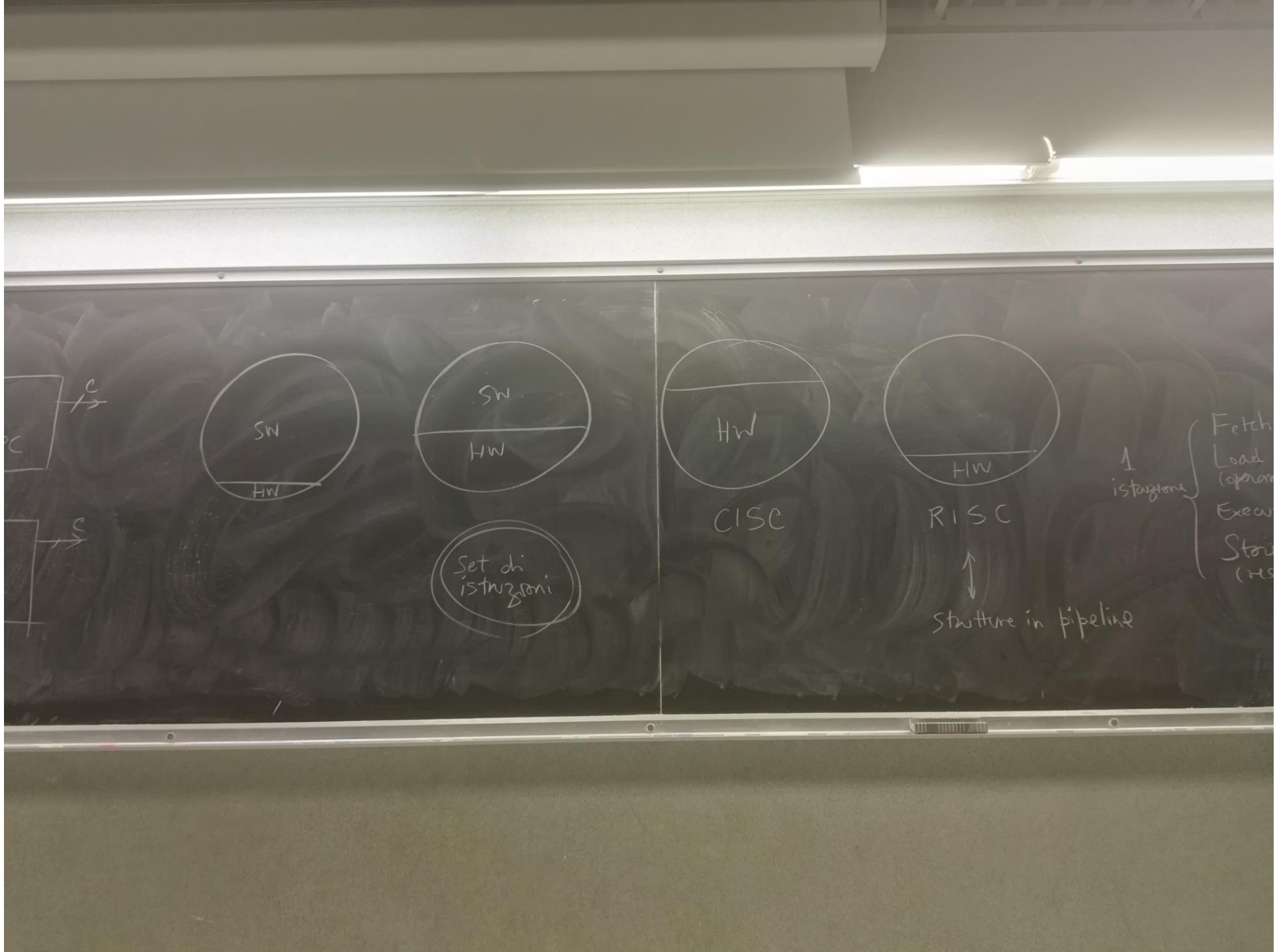
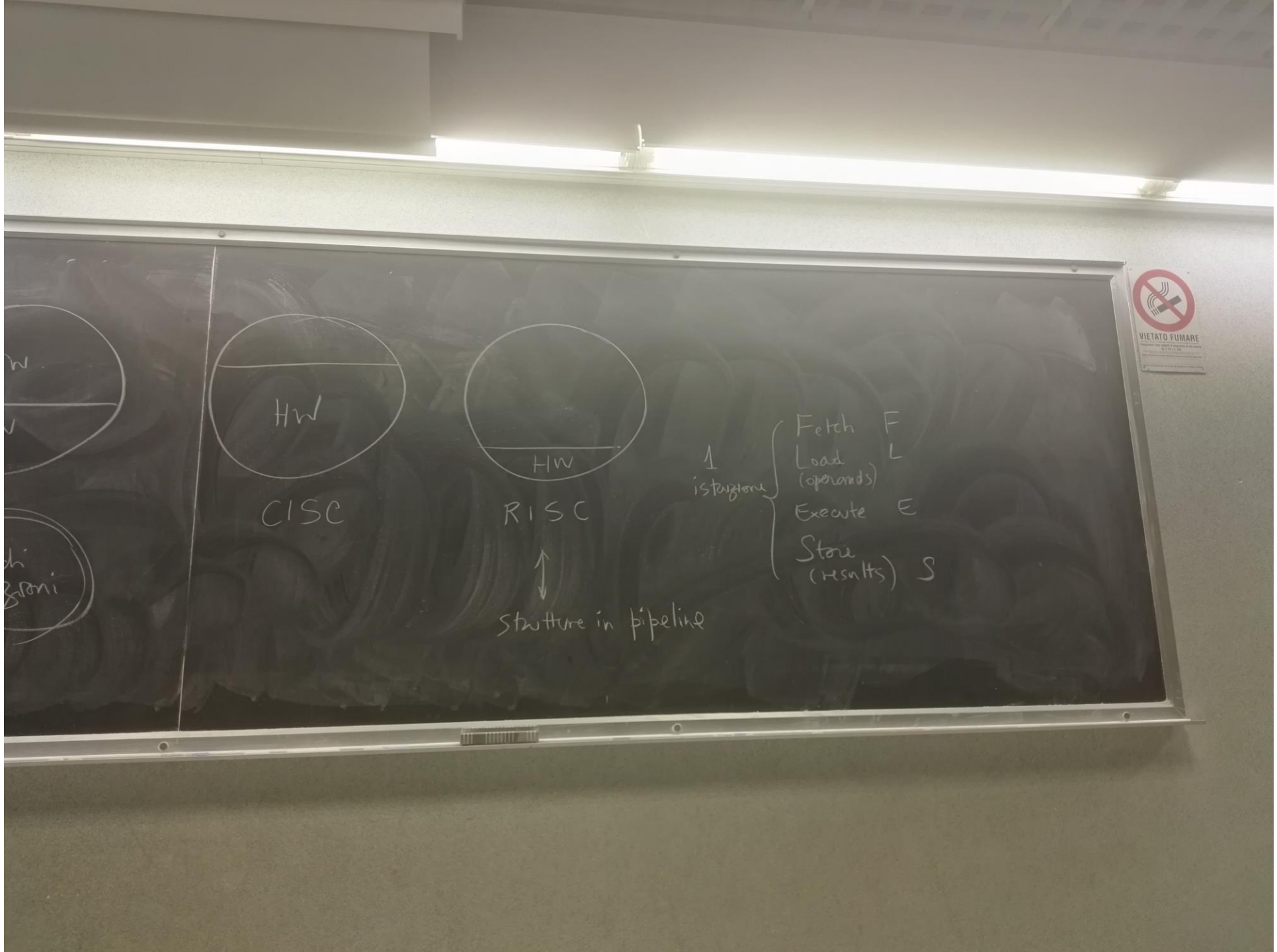
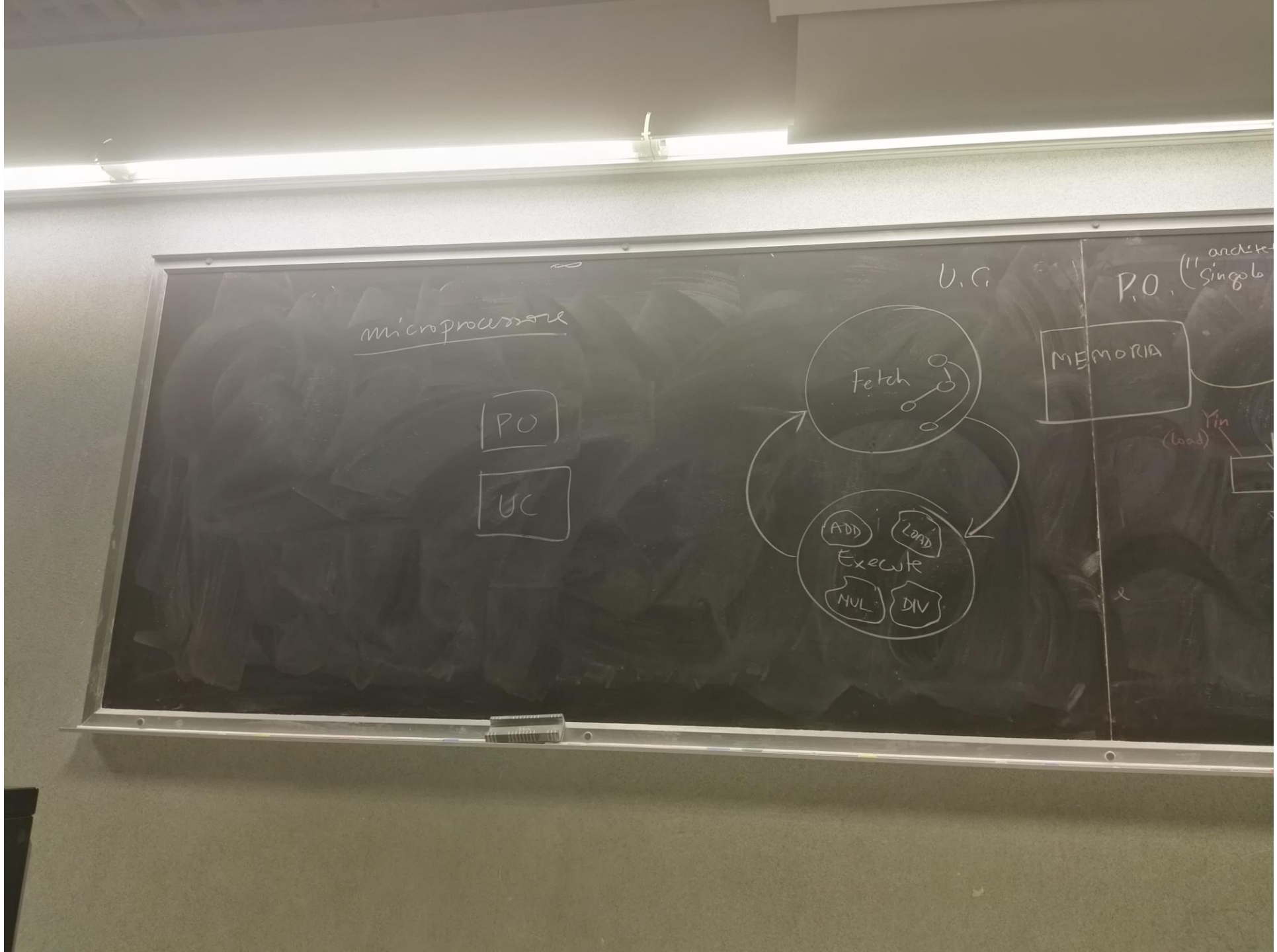
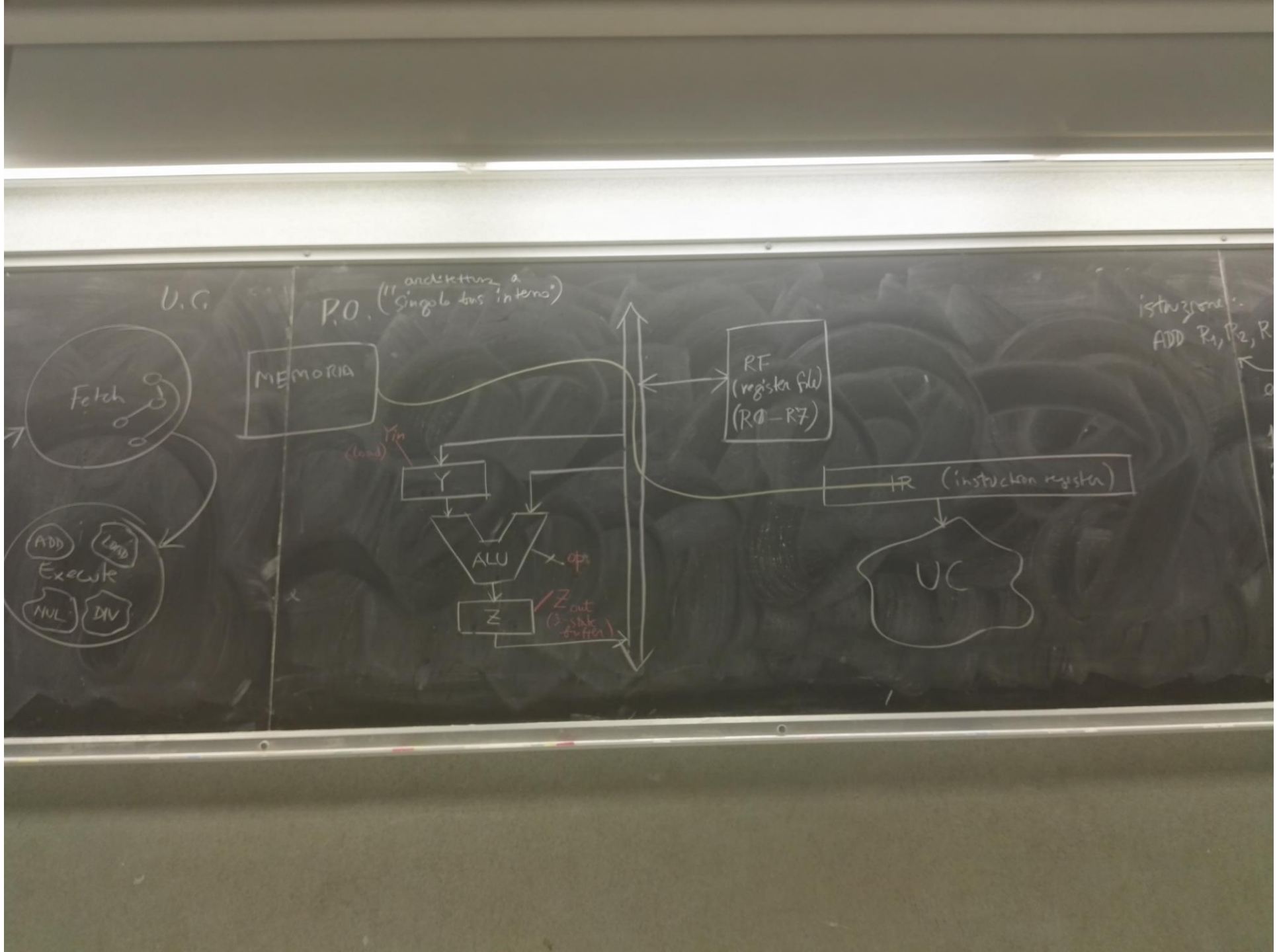

microprocessore
descr. MT (dedicata)
MU Teorica
output MT
istruzione
MU Pratica
istruzioni
competenze hardware
macchine dedicate


A
B
MOLT.
PO/PC
C
A
B
MCD
PO/PC
C
SW
HW
SW
HW
Set di
istruzioni
zze hardware
duplicate


SW
HW
SW
HW
Set di istruzioni
HW
CISC
HW
RISC
Strutture in pipeline
1 istruzione
Fetch
Load
Exec
Stor


HW
CISC
HW
RISC
Strutture in pipeline
1 istruzione
Fetch F
Load (operands) L
Execute E
Store (results) S
VIETATO FUMARE


microprocessore
PO
UC
U.C
Fetch
ADD
LOAD
Execute
MUL
DIV
P.O.
MEMORIA
Yin
(load)


U.C.
Fetch
ADD
LOAD
Execute
MUL
DIV
P.O. ("architettura a singolo bus interno")
MEMORIA
RF
(register file)
(R0 – R7)
Yin
(load)
Y
ALU
opc
Z
Zout
(3 state buffer)
IR (instruction register)
UC
istruzione:
ADD R1, R2, R

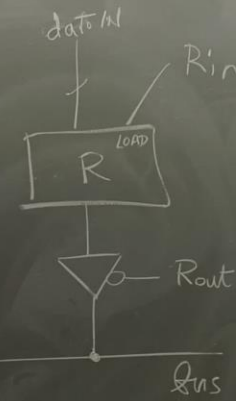
istruzione:

ADD R_1, R_2, R_3 ; $R_3 \leftarrow R_1 + R_2$

esecuzione di:

1. R_1out, Yin
2. R_2out, Add
3. $Zout, R_3in$

(microprogramma)



Tristate (Three-state, 3-state) Buffer