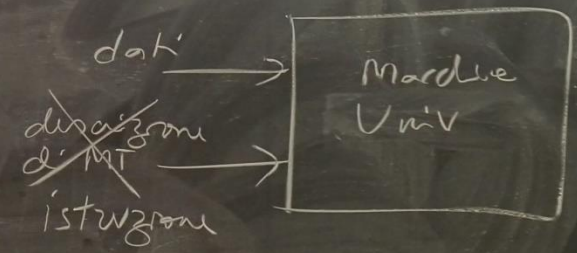
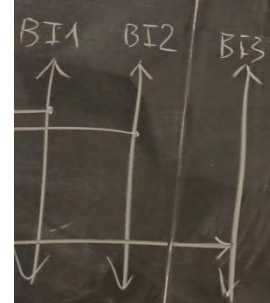
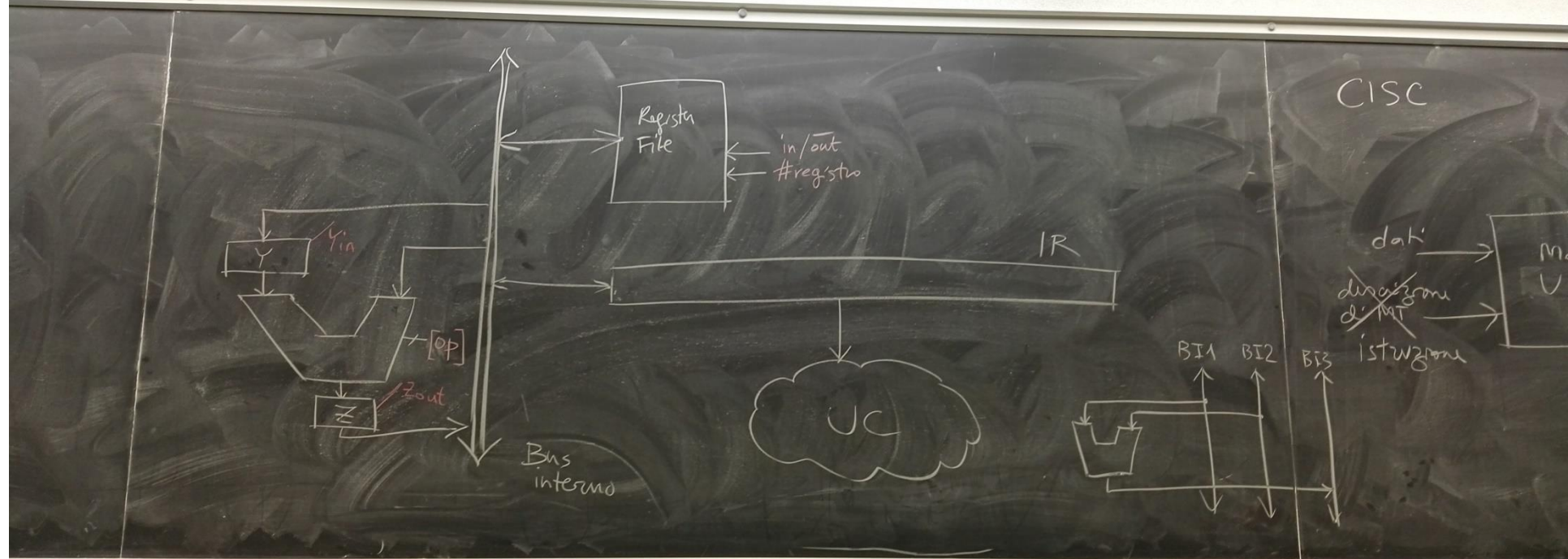
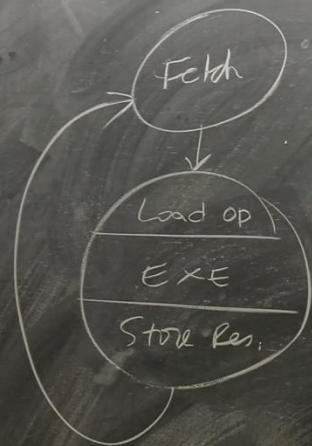


CISC







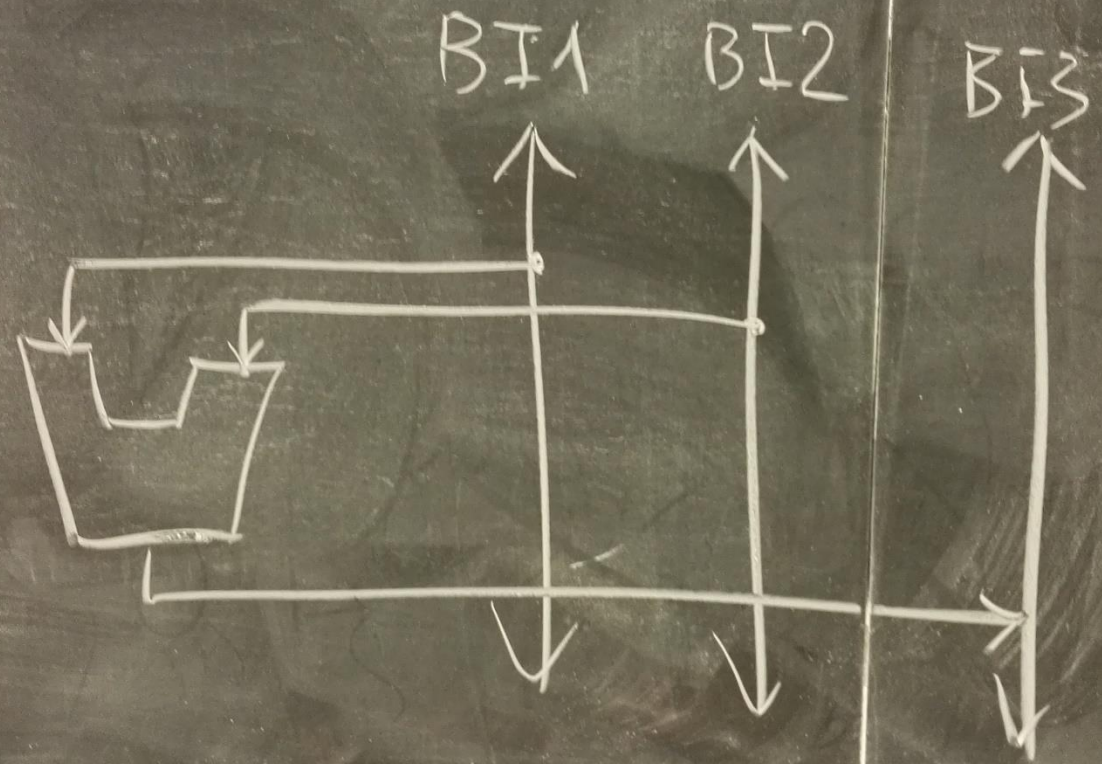
Add R₁, R₂, R₃



1. R₁out, Y_{in}
2. R₂out, ADD
3. Zout, R₃in

SEZIONE
DI CODICE
(istruzioni)

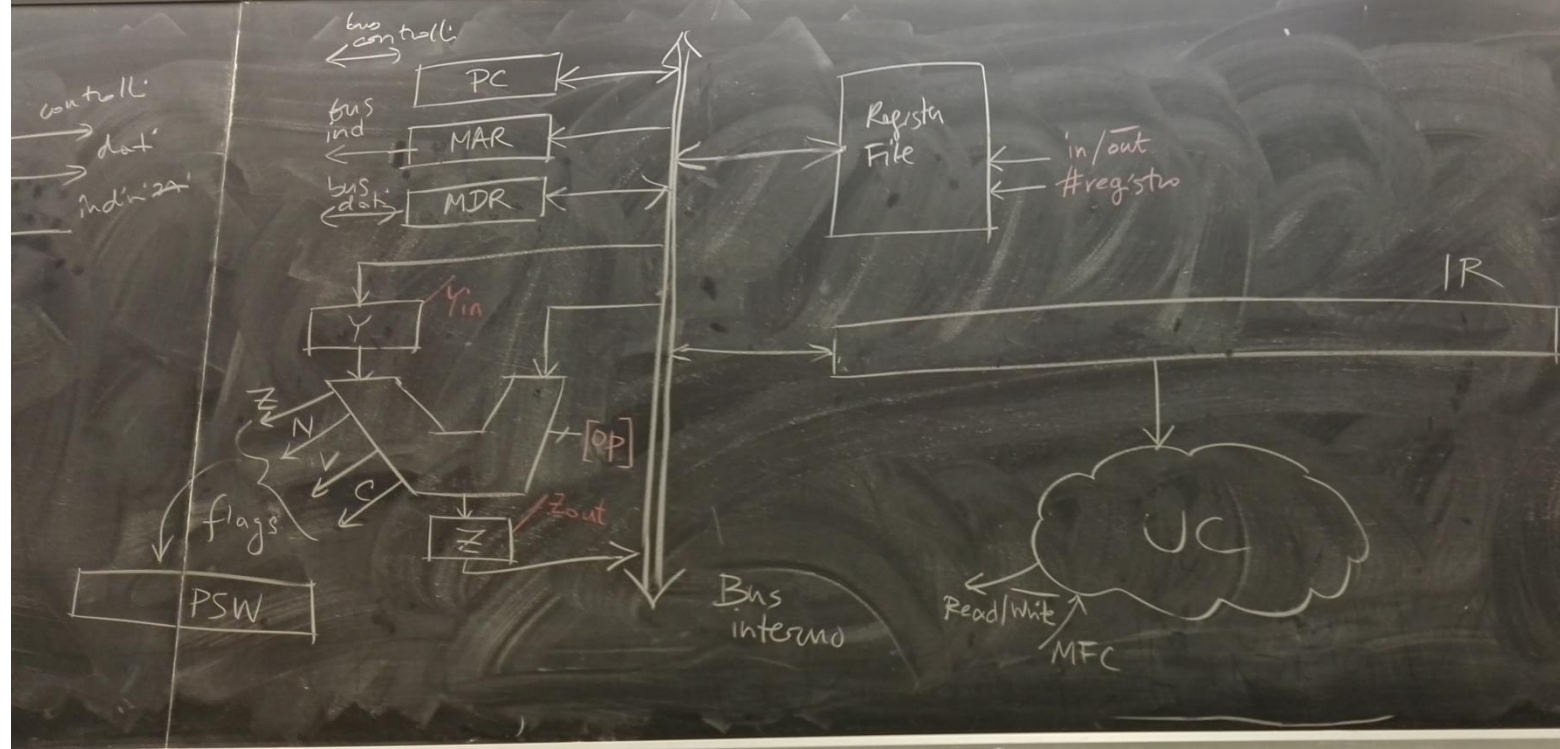
SEZIONE
DATI



5, Low, R) in

Add R₁, A, SUM

Add R₁, A, [R7]



Modi di indirizzamento

ADD op1, op2, op3 ; $op3 \leftarrow op1 + op2$

op _i	{	R1	registro	{ nel RF	
		A	diretto di memoria		{ in mem.
		[R7]	indiretto di registro (con registro R7)		
		1729	immediato (Solo SORGENTE)		



Codifica istruzioni

ADD (R₁, R₂, R₃)



1. (R₁_{out}), Y_{in}
2. (R₂_{out}), ADD
3. Z_{out}, (R₃_{in})

Registra

R0

R1

R7

LOOP PIPPO

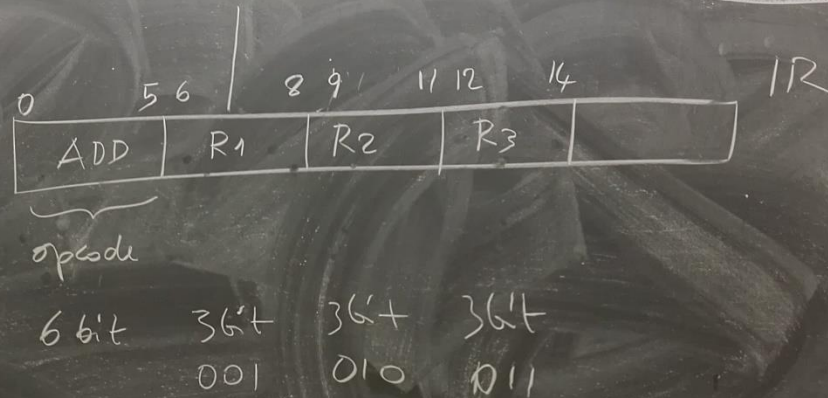


DEC CX

JNZ PIPPO

ADD R₃, R₇, R₆

Registo	Codice registo
R ₀	0 0 0
R ₁	0 0 1
...	...
R ₇	1 1 1

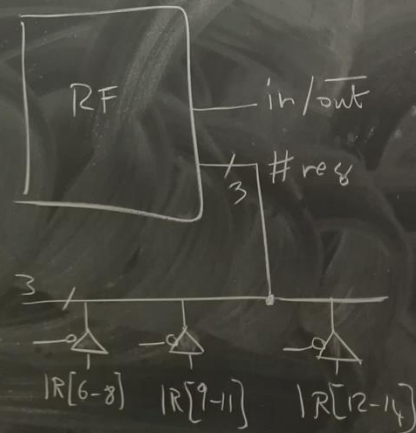


AM "indiretto di memoria" [Var]

→ ADD Reg1, Reg2, RegD

ADD RegS1, RegS2, opD

1. $RF(IR[6-8])_{out}, Y_{in}$
2. $RF(IR[9-11])_{out}, ADD$
3. $Z_{out}, RF(IR[12-14])_{in}$



istruzioni

ADD (R₁, R₂, R₃)

1. (R₁)_{out}, Y_{in}
2. (R₂)_{out}, ADD
3. Z_{out}, (R₃)_{in}

ADD R₃, R₂, R₀

registra	codice registra
R ₀	0 0 0
R ₁	0 0 1
R ₂	1 1 1

0	5 6	2 9	11 12	14	IR
ADD	R ₁	R ₂	R ₃		
opcode					
6 bit	3 bit	3 bit	3 bit		
	001	010	011		

AM "indiretto di memoria" [Var]

ADD R₃, R₂, R₀

1. RF(IR[6-8])_{out}, Y_{in}
2. RF(IR[9-11])_{out}, ADD
3. Z_{out}, RF(IR[12-14])_{in}

ADD